27. The method of claim 23 wherein the semiconductor layer is a polysilicon layer formed by first forming an amorphous silicon layer and annealing the amorphous silicon layer at a temperature within a range of 450° C. to 700° C. for 12 to 70 hours.

28. The method of claim 23 wherein the gate insulating film is sputter formed on a surface of the semiconductor layer.

29. The method of claim 23 wherein the source region and the drain region are formed by implanting phosphorous ions into the semiconductor layer through the gate insulating film.

30. The method of claim 29 wherein the implanted phosphorous ions are radiated with a laser to reduce the resistance level in the semiconductor layer.

31. The method as defined in claim 23 wherein the overlying gate insulator is formed having a lateral thickness, ΔI, which is greater than the lateral offset, ΔL.

32. The method as defined in claim 23 wherein the step of forming the overlying gate insulator by anodic oxidation decreases the width of the gate electrode by about twice the lateral offset, ΔL.--

REMARKS

As discussed hereinafter, new claims 23-32 have been added to initiate an interference with U.S. Patent No. 5,561,075 ('075), the '075 patent being based on a Rule 60 divisional application of U.S. Patent No. 5,383,366 to Nakazawa wherein the claims of the '366 patent are device claims and those of the '075 patent are method claims.

The attention of the Examiner is directed to the filing of an Amendment under 37 CFR 1.607 in Serial No. 08/504,225, the '225 application being the parent of the present Rule 60 divisional application. In particular, the purpose of the foregoing Amendment under 37 CFR 1.607 is to initiate an interference with respect to the device claims of the above-mentioned '366 patent.

Moreover, an Amendment under 37 CFR 1.607 has also been filed in application Serial No. 08/223,823 to also initiate an interference with the foregoing '366 patent. In fact, the claims added to the '225 application are exactly the same as those added to the '823 application. In this regard the issue fee was paid in the '823 application on April 7, 1997, and thus a Petition under 37 CFR 1.313(b)(4) has also been filed to withdraw the '823 application from issue.

Furthermore, upon grant of the foregoing Rule 313(b)(4) Petition and declarations of interferences in the '225 and '823 applications, it has been requested that the foregoing interferences be consolidated into a single interference in view of the fact that the claims added to the '225 and '823 applications are exactly the same.

New claims 23-32 in this Rule 60 divisional application are substantially copied from U.S. Patent No. 5,561,075 to Nakazawa (hereinafter Nakazawa '075 or the '075 patent), a copy of which is submitted herewith. Claims 23-24 and 29-32 are exactly the same as claims 1-2, and 9-12 of the '075 patent and claims 25-28 are generally related to claims 3 and 6-8 of the '075 patent. In accordance with 37 CFR §1.607(a)(5), copied claims 23-32 may be applied to applicant's disclosure as shown in the claims analysis attached thereto as Exhibit A.

In accordance with 37 CFR §1.607(a)(2), applicant presents the following proposed count 1, wherein claim 1 of the '075 patent and claim 23 submitted herewith each correspond exactly to count 1:

1. A method of manufacturing an active matrix panel in which data signals are supplied to liquid crystal layers through a plurality of thin film transistors arranged in a matrix of pixels, gate lines and data lines being coupled to each thin film transistor, said method comprising the steps of:

forming a semiconductor layer on a substrate;

forming a gate insulating film on said semiconductor layer;

forming a gate electrode above said gate insulating film and a gate line in electrical contact with said gate electrode;

forming a source region and a drain region in said semiconductor layer by adding impurities thereto as donors or acceptors using said gate electrode as a self alignment mask;

simultaneously forming an overlying gate insulator on a top and sidewalls of said gate electrode and said gate line by anodic oxidation of said gate electrode and said gate line to reduce the dimensions of said gate electrode and said gate line and simultaneously form a lateral offset, ΔL, from said source region and said drain region to the sidewalls of said gate electrode; and

forming a data line in electrical contact with said source region and crossing over said gate line at a cross-over location, wherein said overlying gate insulator is located between said data line and said gate line at said cross-over location to insulate said data line from said gate line.

With respect to the foregoing, the attention of the Examiner is directed to the fact that, during the prosecution of application Serial No. 07/880,120 (a predecessor application upon which the '075 patent is based), the party Nakazawa filed a verified English translation of one of their Japanese priority applications on July 13, 1994 in order to avoid a rejection under 35 U.S.C. § 102 based on U.S. Patent Number 5,289,030, which patent

issued on a predecessor application of the subject application. In particular, the party Nakazawa attempted to obtain a Japanese filing date earlier than the effective U.S. filing date of the subject application. However, as demonstrated herein and below, the present applicant is entitled to an earlier Japanese filing date than the earliest Japanese filing date of the party Nakazawa with respect to at least claims 23, 25-29, and 31-32.

Verified English translations of the Japanese priority applications (Nos. 3-65418 filed March 6, 1991 and 3-135569 filed May 11, 1991) for the present application are submitted herewith. Newly presented claims 23-32 can be read on these priority applications as shown in Exhibit B. As can be seen, applicant is entitled to the March 6, 1991 priority date for at least claims 23, 25-29 and 31-32. Since applicant's March 6, 1991 priority date is earlier than the May 8, 1991 priority date of the '366 patent, applicant respectfully requests that it be designated senior priority in a declaration of the interference.

Respectfully submitted,

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PENDING CLAIMS	SUPPORT IN JAPANESE PRIORITY APPLICATION 3-65418 (FILED MARCH 6, 1991) OR JAPANESE PRIORITY APPLICATION 3-135569 (FILED MAY 11, 1991)
23. A method of manufacturing an active matrix panel in which data signals are supplied to liquid crystal layers through a plurality of thin film transistors arranged in a matrix of pixels, gate lines and data lines being coupled to each thin film transistor, said method comprising the steps of:	(JP 3-65418); Paragraphs [0022] and [0023]; Figure 4 Figure 4 shows an active matrix liquid crystal display circuit. Data signals are supplied to liquid crystal layers through a plurality of thin film transistors 21, 22 arranged in a matrix of pixels. Gate lines and data lines (such as gate line 50 and data lines 52 and 53) are connected to each transistor.
forming a semiconductor layer on a substrate;	(JP 3-65418); Paragraph [0026]; Figure 3A A semiconductor (silicon) layer is formed on substrate 1.
forming a gate insulating film on said semiconductor layer;	(JP 3-65418); Paragraph [0040]; Figure 3B A gate insulating film 27 is formed on the semiconductor (silicon) layer as shown in Figure 3B.
forming a gate electrode above said gate insulating film and a gate line in electrical contact with said gate electrode;	(JP 3-65418); Paragraphs [0018] and [0041]; Figures 3B and 4 Gate electrode 25 is formed above gate insulating film 27 (Figure 3B) and gate line 50 is formed in electrical contact with gate electrode 25 (Figure 4).
forming a source region and a drain region in said semiconductor layer by adding impurities thereto as donors or acceptors using said gate electrode as a self alignment mask;	(JP 3-65418); Paragraphs [0039], [0042]-[0043], [0047], and [0065]; Figures 3D Source region 35 and drain region 33 are formed in the semiconductor (silicon) layer by adding either boron (acceptor) or phosphorous (donor) impurities, using the gate electrode as a self-alignment mask as discussed in paragraphs [0047] and [0065].
simultaneously forming an overlying gate insulator on a top and sidewalls of said gate electrode and said gate line by anodic oxidation of said gate electrode and said gate line to reduce the dimensions of said gate electrode and said gate line and simultaneously form a lateral offset, ΔL, from said source region and said drain region to the sidewalls of said gate electrode; and	(JP 3-65418); Paragraphs [0016], [0018], [0042]-[0043], [0050]; Figures 1, 3E and 3G As clearly illustrated in Figure 1 source and drain regions 3 are laterally offset by a distance L from each of the adjacent sidewalls of the gate electrode 8, which is covered with aluminum oxide 10. Similarly, in Figure 3G, source region 35 and drain region 33 both have a lateral offset from the side edges of gate electrode 25, which is covered by aluminum oxide layer 40 formed by anodic oxidation. As is further discussed with respect to the following clause of this claim, paragraph [0018] states that the same anodic oxide film covers both the gate electrode and gate wiring. Therefore, the anodic oxide film formed on the gate electrode and the gate line is formed at the same time. The anodic oxidation process necessarily must reduce the dimensions of the gate electrode as stated, for example, in column 3, lines 44-55 of U.S. Patent 5,583,366.

PENDING CLAIMS	SUPPORT IN JAPANESE PRIORITY APPLICATION 3-65418 (FILED MARCH 6, 1991) OR JAPANESE PRIORITY APPLICATION 3-135569 (FILED MAY 11, 1991)
forming a data line in electrical contact with said source region and crossing over said gate line at a cross-over location, wherein said overlying gate insulator is located between said data line and said gate line at said cross-over location to insulate said data line from said gate line.	(JP 3-65418); Paragraphs [0018], [0041], and [0052]; Figures 3B and 3G Data line 53 is coupled to thin film transistor 22, and crosses over gate line 50 at a cross-over location, as shown in Figure 4. Paragraph [0018] of the specification supports this limitation by disclosing that "stereoscopic wirings can be easily made on this aluminum oxide film by crossing wirings of another wiring such as the source electrode . . . ." (Emphasis added). Thus, the aluminum oxide film formed on the gate electrode is the same aluminum oxide film that insulates the gate electrode 50 from the source line 53, which crosses over the aluminum oxide. Since the aluminum oxide film is formed both on the gate electrodes 25, 26 and gate line 50, paragraph [0018] clearly discloses that another wiring, such as the source electrode wiring 53, crosses the gate line at a cross-over location. Also see paragraph [0063] in this regard.
24. The method of claim 23 wherein said gate electrode is comprised of tantalum, and wherein said overlying gate insulator comprises tantalum oxide.	(JP 3-135569); Paragraphs [0037] and [0040] Paragraph [0037] discloses that the gate electrode could be comprised of tantalum. Paragraph [0040] discloses that anodic oxidation of the gate electrode is performed, which would necessarily result in tantalum oxide being formed.
25. The method of claim 23 wherein said gate electrode is selected from the group consisting of tantalum and aluminum.	(JP 3-65418); Paragraphs [0041] and [0050]; Figures 3B and 3E As disclosed in paragraph [0041], gate electrode 25 is formed from aluminum (Figure 3B). Aluminum oxide is formed around gate electrode 25 by anodic oxidation (paragraph [0050]). (JP 3-135569); Paragraphs [0037] and [0040] Paragraph [0037] discloses that the gate electrode could be comprised of tantalum. Paragraph [0040] discloses that anodic oxidation of the gate electrode is performed, which would necessarily result in tantalum oxide being formed.
26. The method of claim 23 wherein the semiconductor layer is a silicon layer formed by decomposing a silane gas using CVD.	(JP 3-65418); Paragraphs [0026]-[0028] The semiconductor layer is silicon formed by decomposing monosilane, disilane, or trisilane using either plasma CVD or low pressure CVD.

PENDING CLAIMS	SUPPORT IN JAPANESE PRIORITY APPLICATION 3-65418 (FILED MARCH 6, 1991) OR JAPANESE PRIORITY APPLICATION 3-135569 (FILED MAY 11, 1991)
27. The method of claim 23 wherein the semiconductor layer is a polysilicon layer formed by first forming an amorphous silicon layer and annealing the amorphous silicon layer at a temperature within a range of 450° C. to 700° C. for 12 to 70 hours.	(JP 3-65418); Paragraphs [0031]-[0033] As described in paragraph [0031], a deposited amorphous silicon film is heated at a temperature of 450-700 °C for 12-70 hours to increase the crystallinity of the film (paragraph [0033]).
28. The method of claim 23 wherein the gate insulating film is sputter formed on a surface of the semiconductor layer.	(JP 3-65418); Paragraphs [0026]-[0027]
29. The method of claim 23 wherein the source region and the drain region are formed by implanting phosphorous ions into the semiconductor layer through the gate insulating film.	(JP 3-65418); Paragraphs [0043]-[0044] Source 35 and drain 33 are formed from implanting phosphorous through gate insulating film 27 as described in paragraphs [0043]-[0044].
30. The method of claim 29 wherein the implanted phosphorous ions are radiated with a laser to reduce the resistance level in the semiconductor layer.	(JP 3-135569); Paragraphs [0022] and [0044] Paragraphs [0022] and [0044] both disclose laser irradiation of source/drain regions including phosphorous to activate these regions and thus reduce the resistance level in the semiconductor layer.
31. The method as defined in claim 23 wherein the overlying gate insulator is formed having a lateral thickness, ΔI, which is greater than the lateral offset, ΔL.	(JP 3-65418); Paragraphs [0016], [0042]-[0043], [0050]; Figures 1, 3E and 3G During the process described with respect to the formation of the device, source region 35 and drain region 33 are formed (paragraphs [0042]-[0043]) before anodic oxide coating 40 is formed (paragraph [0050]). The process described must necessarily result in a thickness of the oxide layer being greater than the lateral offset distance L between source and drain regions and the adjacent edge of the gate electrode. That is, since the source and drain regions are formed using the gate electrode as a mask, and the gate electrode is subsequently anodically oxidized, the thickness of the oxide layer will inherently be greater than the lateral offset distance L.

PENDING CLAIMS	SUPPORT IN JAPANESE PRIORITY APPLICATION 3-65418 (FILED MARCH 6, 1991) OR JAPANESE PRIORITY APPLICATION 3-135569 (FILED MAY 11, 1991)
32. The method as defined in claim 23 wherein the step of forming the overlying gate insulator by anodic oxidation decreases the width of the gate electrode by about twice the lateral offset, ΔL.	The claimed reduction in width of the gate electrode is an inherent result of the described process. That is, source and drain regions are formed using the gate electrode as a mask, and the gate electrode is subsequently anodically oxidized and reduced in width as discussed in connection with claim 1 above. Since the lateral offset is defined to be the distance from the source region and the drain region to the sidewalls of the gate electrode, and this distance is equal to the amount of reduction in the size of the gate electrode on either side, the gate electrode will necessarily be reduced by about twice the lateral offset, ΔL.

PENDING CLAIMS	SUPPORT IN U.S. SERIAL NUMBER 08/504,225
23. A method of manufacturing an active matrix panel in which data signals are supplied to liquid crystal layers through a plurality of thin film transistors arranged in a matrix of pixels, gate lines and data lines being coupled to each thin film transistor, said method comprising the steps of:	Page 15, line 26 - Page 16, line 13; Figure 4 Figure 4 shows an active matrix liquid crystal display circuit. Data signals are supplied to liquid crystal layers through a plurality of thin film transistors 21, 22 arranged in a matrix of pixels. Gate lines and data lines (such as gate line 50 and data lines 52 and 53) are connected to each transistor.
forming a semiconductor layer on a substrate;	Page 16, line 27 - page 17, line 8; Figure 3A A semiconductor (silicon) layer is formed on substrate 1.
forming a gate insulating film on said semiconductor layer;	Page 21, lines 7-13; Figure 3B A gate insulating film 27 is formed on the semiconductor (silicon) layer as shown in Figure 3B.
forming a gate electrode above said gate insulating film and a gate line in electrical contact with said gate electrode;	Page 6, line 22 - Page 7, line 4; Page 21, lines 14-18; Figures 3B and 4 Gate electrode 25 is formed above gate insulating film 27 (Figure 3B) and gate line 50 is formed in electrical contact with gate electrode 25 (Figure 4).
forming a source region and a drain region in said semiconductor layer by adding impurities thereto as donors or acceptors using said gate electrode as a self alignment mask;	Page 21, lines 2-6 and lines 19-24; Page 22, lines 6-11; and Page 37, line 29 - Page 38, line 5; Figures 3D Source region 35 and drain region 33 are formed in the semiconductor (silicon) layer by adding either boron (acceptor) or phosphorous (donor) impurities, using the gate electrode as a self-alignment mask.
simultaneously forming an overlying gate insulator on a top and sidewalls of said gate electrode and said gate line by anodic oxidation of said gate electrode and said gate line to reduce the dimensions of said gate electrode and said gate line and simultaneously form a lateral offset, ΔL, from said source region and said drain region to the sidewalls of said gate electrode; and	Page 5, line 24 - Page 6, line 13; Page 6, line 22 - Page 7, line 4; Page 21, lines 19-24; Page 22, lines 23-30; Figures 1, 3E and 3G As clearly illustrated in Figure 1 source and drain regions 3 are laterally offset by a distance L from each of the adjacent sidewalls of the gate electrode 8, which is covered with aluminum oxide 10. Similarly, in Figure 3G, source region 35 and drain region 33 both have a lateral offset from the side edges of gate electrode 25, which is covered by aluminum oxide layer 40 formed by anodic oxidation. As is further discussed with respect to the following clause of this claim, pages 6-7 state that the same anodic oxide film covers both the gate electrode and gate wiring. Therefore, this anodic oxide film formed on the gate electrode and the gate line is formed at the same time. The anodic oxidation process necessarily must reduce the dimensions of the gate electrode as stated, for example, in column 3, lines 44-55 of U.S. Patent 5,583,366.

PENDING CLAIMS	SUPPORT IN U.S. SERIAL NUMBER 08/504,225
forming a data line in electrical contact with said source region and crossing over said gate line at a cross-over location, wherein said overlying gate insulator is located between said data line and said gate line at said cross-over location to insulate said data line from said gate line.	Page 6, line 22 - Page 7, line 4; Page 21, lines 14-18; and Page 24, lines 7-11; Figures 3B and 3G Data line 53 is coupled to thin film transistor 22, and crosses over gate line 50 at a cross-over location, as shown in Figure 4. Pages 6-7 of the specification supports this limitation by disclosing that "other wiring, e.g., a wiring for the source electrode, may be crossed over this aluminum oxide film to establish a three-dimensional wiring . . . ." (Emphasis added). Thus, the aluminum oxide film formed on the gate electrode is the same aluminum oxide film that insulates the gate electrode 50 from the source line 53, which crosses over the aluminum oxide. Since the aluminum oxide film is formed both on the gate electrodes 25, 26 and gate line 50, page 7 clearly discloses that another wiring, such as the source electrode wiring 53, crosses the gate line at a cross-over location.
24. The method of claim 23 wherein said gate electrode is comprised of tantalum, and wherein said overlying gate insulator comprises tantalum oxide.	Page 28, lines 5-8 and 21-31 Page 28 discloses that the gate electrode could be comprised of tantalum and discloses that anodic oxidation of the gate electrode is performed, which would necessarily result in tantalum oxide being formed.
25. The method of claim 23 wherein said gate electrode is selected from the group consisting of tantalum and aluminum.	Page 21, lines 14-18, Page 22, lines 23-30, and Page 28, lines 5-8 and 21-31; Figures 3B and 3E As discussed on Pages 21 and 22, gate electrode 25 is formed from aluminum (Figure 3B). Aluminum oxide is formed around gate electrode 25 by anodic oxidation. Page 28 discloses that the gate electrode could be comprised of tantalum and discloses that anodic oxidation of the gate electrode is performed, which would necessarily result in tantalum oxide being formed.
26. The method of claim 23 wherein the semiconductor layer is a silicon layer formed by decomposing a silane gas using CVD.	Page 16, line 27 - Page 17, line 21 The semiconductor layer is silicon formed by decomposing monosilane, disilane, or trisilane using either plasma CVD or low pressure CVD.
27. The method of claim 23 wherein the semiconductor layer is a polysilicon layer formed by first forming an amorphous silicon layer and annealing the amorphous silicon layer at a temperature within a range of 450° C. to 700° C. for 12 to 70 hours.	Page 18, line 20 - page 19, line 18 As described on pages 18-19, a deposited amorphous silicon film is heated at a temperature of 450-700 °C for 12-70 hours to increase the crystallinity of the film.
28. The method of claim 23 wherein the gate insulating film is sputter formed on a surface of the semiconductor layer.	Page 16, line 31 - Page 17, line 16

PENDING CLAIMS	SUPPORT IN U.S. SERIAL NUMBER 08/504,225
29. The method of claim 23 wherein the source region and the drain region are formed by implanting phosphorous ions into the semiconductor layer through the gate insulating film.	Page 21, lines 22-29 Source 35 and drain 33 are formed from implanting phosphorous through gate insulating film 27.
30. The method of claim 29 wherein the implanted phosphorous ions are radiated with a laser to reduce the resistance level in the semiconductor layer.	Page 11, lines 8-20 and Page 30, lines 2-14 Page 11 and 30 disclose laser irradiation of source/drain regions including phosphorous to activate these regions and thus reduce the resistance level in the semiconductor layer.
31. The method as defined in claim 23 wherein the overlying gate insulator is formed having a lateral thickness, ΔI, which is greater than the lateral offset, ΔL.	Page 5, line 24 - Page 6, line 13; Page 21, lines 19-24; Page 22, lines 23-30; Figures 1, 3E and 3G During the process described with respect to the formation of the device, source region 35 and drain region 33 are formed before anodic oxide coating 40 is formed. The process described must necessarily result in a thickness of the oxide layer being greater than the lateral offset distance L between source and drain regions and the adjacent edge of the gate electrode. That is, since the source and drain regions are formed using the gate electrode as a mask, and the gate electrode is subsequently anodically oxidized, the thickness of the oxide layer will inherently be greater than the lateral offset distance L.
32. The method as defined in claim 23 wherein the step of forming the overlying gate insulator by anodic oxidation decreases the width of the gate electrode by about twice the lateral offset, ΔL.	The claimed reduction in width of the gate electrode is an inherent result of the described process. That is, source and drain regions are formed using the gate electrode as a mask, and the gate electrode is subsequently anodically oxidized and reduced in width as discussed in connection with claim 1 above. Since the lateral offset is defined to be the distance from the source region and the drain region to the sidewalls of the gate electrode, and this distance is equal to the amount of reduction in the size of the gate electrode on either side, the gate electrode will necessarily be reduced by about twice the lateral offset, ΔL.

PENDING CLAIMS	SUPPORT IN U.S. SERIAL NUMBER 08/504,225
23. A method of manufacturing an active matrix panel in which data signals are supplied to liquid crystal layers through a plurality of thin film transistors arranged in a matrix of pixels, gate lines and data lines being coupled to each thin film transistor, said method comprising the steps of:	Page 15, line 26 - Page 16, line 13; Figure 4 Figure 4 shows an active matrix liquid crystal display circuit. Data signals are supplied to liquid crystal layers through a plurality of thin film transistors 21, 22 arranged in a matrix of pixels. Gate lines and data lines (such as gate line 50 and data lines 52 and 53) are connected to each transistor.
forming a semiconductor layer on a substrate;	Page 16, line 27 - page 17, line 8; Figure 3A A semiconductor (silicon) layer is formed on substrate 1.
forming a gate insulating film on said semiconductor layer;	Page 21, lines 7-13; Figure 3B A gate insulating film 27 is formed on the semiconductor (silicon) layer as shown in Figure 3B.
forming a gate electrode above said gate insulating film and a gate line in electrical contact with said gate electrode;	Page 6, line 22 - Page 7, line 4; Page 21, lines 14-18; Figures 3B and 4 Gate electrode 25 is formed above gate insulating film 27 (Figure 3B) and gate line 50 is formed in electrical contact with gate electrode 25 (Figure 4).
forming a source region and a drain region in said semiconductor layer by adding impurities thereto as donors or acceptors using said gate electrode as a self alignment mask;	Page 21, lines 2-6 and lines 19-24; Page 22, lines 6-11; and Page 37, line 29 - Page 38, line 5; Figures 3D Source region 35 and drain region 33 are formed in the semiconductor (silicon) layer by adding either boron (acceptor) or phosphorous (donor) impurities, using the gate electrode as a self-alignment mask.
simultaneously forming an overlying gate insulator on a top and sidewalls of said gate electrode and said gate line by anodic oxidation of said gate electrode and said gate line to reduce the dimensions of said gate electrode and said gate line and simultaneously form a lateral offset, ΔL, from said source region and said drain region to the sidewalls of said gate electrode; and	Page 5, line 24 - Page 6, line 13; Page 6, line 22 - Page 7, line 4; Page 21, lines 19-24; Page 22, lines 23-30; Figures 1, 3E and 3G As clearly illustrated in Figure 1 source and drain regions 3 are laterally offset by a distance L from each of the adjacent sidewalls of the gate electrode 8, which is covered with aluminum oxide 10. Similarly, in Figure 3G, source region 35 and drain region 33 both have a lateral offset from the side edges of gate electrode 25, which is covered by aluminum oxide layer 40 formed by anodic oxidation. As is further discussed with respect to the following clause of this claim, pages 6-7 state that the same anodic oxide film covers both the gate electrode and gate wiring. Therefore, this anodic oxide film formed on the gate electrode and the gate line is formed at the same time. The anodic oxidation process necessarily must reduce the dimensions of the gate electrode as stated, for example, in column 3, lines 44-55 of U.S. Patent 5,583,366.

PENDING CLAIMS	SUPPORT IN U.S. SERIAL NUMBER 08/504,225
forming a data line in electrical contact with said source region and crossing over said gate line at a cross-over location, wherein said overlying gate insulator is located between said data line and said gate line at said cross-over location to insulate said data line from said gate line.	Page 6, line 22 - Page 7, line 4; Page 21, lines 14-18; and Page 24, lines 7-11; Figures 3B and 3G Data line 53 is coupled to thin film transistor 22, and crosses over gate line 50 at a cross-over location, as shown in Figure 4. Pages 6-7 of the specification supports this limitation by disclosing that "other wiring, e.g., a wiring for the source electrode, may be crossed over this aluminum oxide film to establish a three-dimensional wiring . . . ." (Emphasis added). Thus, the aluminum oxide film formed on the gate electrode is the same aluminum oxide film that insulates the gate electrode 50 from the source line 53, which crosses over the aluminum oxide. Since the aluminum oxide film is formed both on the gate electrodes 25, 26 and gate line 50, page 7 clearly discloses that another wiring, such as the source electrode wiring 53, crosses the gate line at a cross-over location.
24. The method of claim 23 wherein said gate electrode is comprised of tantalum, and wherein said overlying gate insulator comprises tantalum oxide.	Page 28, lines 5-8 and 21-31 Page 28 discloses that the gate electrode could be comprised of tantalum and discloses that anodic oxidation of the gate electrode is performed, which would necessarily result in tantalum oxide being formed.
25. The method of claim 23 wherein said gate electrode is selected from the group consisting of tantalum and aluminum.	Page 21, lines 14-18, Page 22, lines 23-30, and Page 28, lines 5-8 and 21-31; Figures 3B and 3E As discussed on Pages 21 and 22, gate electrode 25 is formed from aluminum (Figure 3B). Aluminum oxide is formed around gate electrode 25 by anodic oxidation. Page 28 discloses that the gate electrode could be comprised of tantalum and discloses that anodic oxidation of the gate electrode is performed, which would necessarily result in tantalum oxide being formed.
26. The method of claim 23 wherein the semiconductor layer is a silicon layer formed by decomposing a silane gas using CVD.	Page 16, line 27 - Page 17, line 21 The semiconductor layer is silicon formed by decomposing monosilane, disilane, or trisilane using either plasma CVD or low pressure CVD.
27. The method of claim 23 wherein the semiconductor layer is a polysilicon layer formed by first forming an amorphous silicon layer and annealing the amorphous silicon layer at a temperature within a range of 450° C. to 700° C. for 12 to 70 hours.	Page 18, line 20 - page 19, line 18 As described on pages 18-19, a deposited amorphous silicon film is heated at a temperature of 450-700 °C for 12-70 hours to increase the crystallinity of the film.
28. The method of claim 23 wherein the gate insulating film is sputter formed on a surface of the semiconductor layer.	Page 16, line 31 - Page 17, line 16

PENDING CLAIMS	SUPPORT IN U.S. SERIAL NUMBER 08/504,225
29. The method of claim 23 wherein the source region and the drain region are formed by implanting phosphorous ions into the semiconductor layer through the gate insulating film.	Page 21, lines 22-29 Source 35 and drain 33 are formed from implanting phosphorous through gate insulating film 27.
30. The method of claim 29 wherein the implanted phosphorous ions are radiated with a laser to reduce the resistance level in the semiconductor layer.	Page 11, lines 8-20 and Page 30, lines 2-14 Page 11 and 30 disclose laser irradiation of source/drain regions including phosphorous to activate these regions and thus reduce the resistance level in the semiconductor layer.
31. The method as defined in claim 23 wherein the overlying gate insulator is formed having a lateral thickness, ΔI, which is greater than the lateral offset, ΔL.	Page 5, line 24 - Page 6, line 13; Page 21, lines 19-24; Page 22, lines 23-30; Figures 1, 3E and 3G During the process described with respect to the formation of the device, source region 35 and drain region 33 are formed before anodic oxide coating 40 is formed. The process described must necessarily result in a thickness of the oxide layer being greater than the lateral offset distance L between source and drain regions and the adjacent edge of the gate electrode. That is, since the source and drain regions are formed using the gate electrode as a mask, and the gate electrode is subsequently anodically oxidized, the thickness of the oxide layer will inherently be greater than the lateral offset distance L.
32. The method as defined in claim 23 wherein the step of forming the overlying gate insulator by anodic oxidation decreases the width of the gate electrode by about twice the lateral offset, ΔL.	The claimed reduction in width of the gate electrode is an inherent result of the described process. That is, source and drain regions are formed using the gate electrode as a mask, and the gate electrode is subsequently anodically oxidized and reduced in width as discussed in connection with claim 1 above. Since the lateral offset is defined to be the distance from the source region and the drain region to the sidewalls of the gate electrode, and this distance is equal to the amount of reduction in the size of the gate electrode on either side, the gate electrode will necessarily be reduced by about twice the lateral offset, ΔL.

PENDING CLAIMS	SUPPORT IN JAPANESE PRIORITY APPLICATION 3-65418 (FILED MARCH 6, 1991) OR JAPANESE PRIORITY APPLICATION 3-135569 (FILED MAY 11, 1991)
23. A method of manufacturing an active matrix panel in which data signals are supplied to liquid crystal layers through a plurality of thin film transistors arranged in a matrix of pixels, gate lines and data lines being coupled to each thin film transistor, said method comprising the steps of:	(JP 3-65418); Paragraphs [0022] and [0023]; Figure 4 Figure 4 shows an active matrix liquid crystal display circuit. Data signals are supplied to liquid crystal layers through a plurality of thin film transistors 21, 22 arranged in a matrix of pixels. Gate lines and data lines (such as gate line 50 and data lines 52 and 53) are connected to each transistor.
forming a semiconductor layer on a substrate;	(JP 3-65418); Paragraph [0026]; Figure 3A A semiconductor (silicon) layer is formed on substrate 1.
forming a gate insulating film on said semiconductor layer;	(JP 3-65418); Paragraph [0040]; Figure 3B A gate insulating film 27 is formed on the semiconductor (silicon) layer as shown in Figure 3B.
forming a gate electrode above said gate insulating film and a gate line in electrical contact with said gate electrode;	(JP 3-65418); Paragraphs [0018] and [0041]; Figures 3B and 4 Gate electrode 25 is formed above gate insulating film 27 (Figure 3B) and gate line 50 is formed in electrical contact with gate electrode 25 (Figure 4).
forming a source region and a drain region in said semiconductor layer by adding impurities thereto as donors or acceptors using said gate electrode as a self alignment mask;	(JP 3-65418); Paragraphs [0039], [0042]-[0043], [0047], and [0065]; Figures 3D Source region 35 and drain region 33 are formed in the semiconductor (silicon) layer by adding either boron (acceptor) or phosphorous (donor) impurities, using the gate electrode as a self-alignment mask as discussed in paragraphs [0047] and [0065].
simultaneously forming an overlying gate insulator on a top and sidewalls of said gate electrode and said gate line by anodic oxidation of said gate electrode and said gate line to reduce the dimensions of said gate electrode and said gate line and simultaneously form a lateral offset, ΔL, from said source region and said drain region to the sidewalls of said gate electrode; and	(JP 3-65418); Paragraphs [0016], [0018], [0042]-[0043], [0050]; Figures 1, 3E and 3G As clearly illustrated in Figure 1 source and drain regions 3 are laterally offset by a distance L from each of the adjacent sidewalls of the gate electrode 8, which is covered with aluminum oxide 10. Similarly, in Figure 3G, source region 35 and drain region 33 both have a lateral offset from the side edges of gate electrode 25, which is covered by aluminum oxide layer 40 formed by anodic oxidation. As is further discussed with respect to the following clause of this claim, paragraph [0018] states that the same anodic oxide film covers both the gate electrode and gate wiring. Therefore, the anodic oxide film formed on the gate electrode and the gate line is formed at the same time. The anodic oxidation process necessarily must reduce the dimensions of the gate electrode as stated, for example, in column 3, lines 44-55 of U.S. Patent 5,583,366.

PENDING CLAIMS	SUPPORT IN JAPANESE PRIORITY APPLICATION 3-65418 (FILED MARCH 6, 1991) OR JAPANESE PRIORITY APPLICATION 3-135569 (FILED MAY 11, 1991)
forming a data line in electrical contact with said source region and crossing over said gate line at a cross-over location, wherein said overlying gate insulator is located between said data line and said gate line at said cross-over location to insulate said data line from said gate line.	(JP 3-65418); Paragraphs [0018], [0041], and [0052]; Figures 3B and 3G Data line 53 is coupled to thin film transistor 22, and crosses over gate line 50 at a cross-over location, as shown in Figure 4. Paragraph [0018] of the specification supports this limitation by disclosing that "stereoscopic wirings can be easily made on this aluminum oxide film by crossing wirings of another wiring such as the source electrode . . . ." (Emphasis added). Thus, the aluminum oxide film formed on the gate electrode is the same aluminum oxide film that insulates the gate electrode 50 from the source line 53, which crosses over the aluminum oxide. Since the aluminum oxide film is formed both on the gate electrodes 25, 26 and gate line 50, paragraph [0018] clearly discloses that another wiring, such as the source electrode wiring 53, crosses the gate line at a cross-over location. Also see paragraph [0063] in this regard.
24. The method of claim 23 wherein said gate electrode is comprised of tantalum, and wherein said overlying gate insulator comprises tantalum oxide.	(JP 3-135569); Paragraphs [0037] and [0040] Paragraph [0037] discloses that the gate electrode could be comprised of tantalum. Paragraph [0040] discloses that anodic oxidation of the gate electrode is performed, which would necessarily result in tantalum oxide being formed.
25. The method of claim 23 wherein said gate electrode is selected from the group consisting of tantalum and aluminum.	(JP 3-65418); Paragraphs [0041] and [0050]; Figures 3B and 3E As disclosed in paragraph [0041], gate electrode 25 is formed from aluminum (Figure 3B). Aluminum oxide is formed around gate electrode 25 by anodic oxidation (paragraph [0050]). (JP 3-135569); Paragraphs [0037] and [0040] Paragraph [0037] discloses that the gate electrode could be comprised of tantalum. Paragraph [0040] discloses that anodic oxidation of the gate electrode is performed, which would necessarily result in tantalum oxide being formed.
26. The method of claim 23 wherein the semiconductor layer is a silicon layer formed by decomposing a silane gas using CVD.	(JP 3-65418); Paragraphs [0026]-[0028] The semiconductor layer is silicon formed by decomposing monosilane, disilane, or trisilane using either plasma CVD or low pressure CVD.

PENDING CLAIMS	SUPPORT IN JAPANESE PRIORITY APPLICATION 3-65418 (FILED MARCH 6, 1991) OR JAPANESE PRIORITY APPLICATION 3-135569 (FILED MAY 11, 1991)
27. The method of claim 23 wherein the semiconductor layer is a polysilicon layer formed by first forming an amorphous silicon layer and annealing the amorphous silicon layer at a temperature within a range of 450° C. to 700° C. for 12 to 70 hours.	(JP 3-65418); Paragraphs [0031]-[0033] As described in paragraph [0031], a deposited amorphous silicon film is heated at a temperature of 450-700 °C for 12-70 hours to increase the crystallinity of the film (paragraph [0033]).
28. The method of claim 23 wherein the gate insulating film is sputter formed on a surface of the semiconductor layer.	(JP 3-65418); Paragraphs [0026]-[0027]
29. The method of claim 23 wherein the source region and the drain region are formed by implanting phosphorous ions into the semiconductor layer through the gate insulating film.	(JP 3-65418); Paragraphs [0043]-[0044] Source 35 and drain 33 are formed from implanting phosphorous through gate insulating film 27 as described in paragraphs [0043]-[0044].
30. The method of claim 29 wherein the implanted phosphorous ions are radiated with a laser to reduce the resistance level in the semiconductor layer.	(JP 3-135569); Paragraphs [0022] and [0044] Paragraphs [0022] and [0044] both disclose laser irradiation of source/drain regions including phosphorous to activate these regions and thus reduce the resistance level in the semiconductor layer.
31. The method as defined in claim 23 wherein the overlying gate insulator is formed having a lateral thickness, ΔI, which is greater than the lateral offset, ΔL.	(JP 3-65418); Paragraphs [0016], [0042]-[0043], [0050]; Figures 1, 3E and 3G During the process described with respect to the formation of the device, source region 35 and drain region 33 are formed (paragraphs [0042]-[0043]) before anodic oxide coating 40 is formed (paragraph [0050]). The process described must necessarily result in a thickness of the oxide layer being greater than the lateral offset distance L between source and drain regions and the adjacent edge of the gate electrode. That is, since the source and drain regions are formed using the gate electrode as a mask, and the gate electrode is subsequently anodically oxidized, the thickness of the oxide layer will inherently be greater than the lateral offset distance L.

PENDING CLAIMS	SUPPORT IN JAPANESE PRIORITY APPLICATION 3-65418 (FILED MARCH 6, 1991) OR JAPANESE PRIORITY APPLICATION 3-135569 (FILED MAY 11, 1991)
32. The method as defined in claim 23 wherein the step of forming the overlying gate insulator by anodic oxidation decreases the width of the gate electrode by about twice the lateral offset, ΔL.	The claimed reduction in width of the gate electrode is an inherent result of the described process. That is, source and drain regions are formed using the gate electrode as a mask, and the gate electrode is subsequently anodically oxidized and reduced in width as discussed in connection with claim 1 above. Since the lateral offset is defined to be the distance from the source region and the drain region to the sidewalls of the gate electrode, and this distance is equal to the amount of reduction in the size of the gate electrode on either side, the gate electrode will necessarily be reduced by about twice the lateral offset, ΔL.